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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PARK, EDWARD K	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 03/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,762	SCHMISSEUR ET AL.	
	Examiner	Art Unit	
	Edward K. Park	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 35 objected to because of the following informalities: the phrase "...wherein the instructions further comprise one or more instructions..." should read "...wherein the one or more instructions further comprise instructions...". Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 9-12, 15-19, 22-26 and 29-33 rejected under 35 U.S.C. 102(b) as being anticipated by Anderson (U.S. 5,898,869). Said claims are rejected in view of amended claims 1, 9, 15, 22, and 29.

Regarding claim 1, Anderson discloses a system comprising: a core processing circuit (13); and a host processing system (11) coupled to the core processing circuit through a host bridge (17), the host processing system comprising: logic to place the core processing circuit in a reset state (column 2, lines 65-66; column 3, lines 6-7); and logic to load a reset vector to one or more registers at a boot address associated with the core processing circuit (column 6, lines 13-15 in view of column 8, lines 7-9; Anderson discloses the reset vector as comprising an "initial program," which

necessarily must be loaded to registers), the reset vector comprising one or more instructions to fetch additional instructions to initialize the core processing circuit upon release from the release state (column 8, lines 24-26; Anderson discloses an included loader program to download a program from host 11 to FLASH memory, which necessarily must include fetching additional instructions).

Regarding claim 2, Anderson discloses the system of claim 1, wherein the registers are formed in a memory (39) coupled to the core processing circuit (31) through a data bus (26).

Regarding claim 3, Anderson discloses the system of claim 1, wherein the host processing system comprises a system memory (39), and wherein the reset vector comprises at least one instruction to fetch data from a system memory (column 2, line 66 through column 3, line 2) coupled to the core processing circuit through the host bridge (17).

Regarding claim 4, Anderson discloses the system of claim 3, wherein the host processing system further comprises logic to set an address translation unit to fetch instructions from the system memory in response to requests from the core processing unit (column 2, lines 48-50, via processor address bus 24).

Regarding claim 5, Anderson discloses the system of claim 3, wherein the host processing system further comprises logic to load the reset vector in the registers while the core processing circuit is in the reset state (column 6, lines 5-7), and wherein the core processing circuit comprises logic to initiate the system memory in response to execution of the reset vector upon release from the reset state (column 6, lines 13-15).

Anderson does not explicitly disclose the initiation of one or more write bus transactions at an address translation unit nor one or more read bus transactions at the address translation unit addressed to the system memory, however said transactions would necessarily have to be present in order for the host processing system to properly communicate with the core processing circuit.

Regarding claim 6, Anderson discloses the system of claim 1, wherein the host processing system further comprises logic to release the core processing circuit from the reset state in response to loading the reset vector at the boot address (column 2, lines 37-39).

Regarding claim 9, Anderson discloses a method comprising: having a host processing system place a core processing unit (13) in a reset state (column 2, lines 65-66; column 3, lines 6-7); and loading a reset vector to one or more registers at a boot address associated with the core processing circuit (column 6, lines 13-15 in view of column 8, lines 7-9; Anderson discloses the reset vector as comprising an "initial program," which necessarily must be loaded to registers), the reset vector comprising one or more instructions to fetch additional instructions from a system memory (column 8, lines 24-26; Anderson discloses an included loader program to download a program from host 11 to FLASH memory, which necessarily must include fetching additional instructions) coupled to the core processing circuit through a host bridge (17) of a host processing system (11).

Regarding claim 10, Anderson discloses the method of claim 9, the method further comprising loading the reset vector to a boot address in registers formed in a memory (39) coupled to the core processing circuit (31) through a data bus (26).

Regarding claim 11, Anderson discloses the method of claim 9, wherein the method further comprises setting an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit (column 2, lines 48-50, via processor address bus 24).

Regarding claim 12, Anderson discloses the method of claim 9, wherein the method further comprises: loading the reset vector in the registers while the core processing circuit is in the reset state (column 6, lines 5-7); and initiating the system memory in response to execution of the reset vector upon release of the core processing circuit from the reset state (column 6, lines 13-15). Anderson does not explicitly disclose initiating of one or more write bus transactions at an address translation unit nor one or more read bus transactions at the address translation unit addressed to the system memory, however said transactions would necessarily have to be present in order for the host processing system to properly communicate with the core processing circuit.

Regarding claim 15, Anderson discloses a method comprising: having a host processing system place a core processing circuit (13) in a reset state (column 2, lines 65-66; column 3, lines 6-7); and loading instructions from a system memory of a host processing system to one or more registers at a boot address associated with the core processing circuit (column 6, lines 13-15 in view of column 8, lines 7-9; Anderson

discloses the reset vector as comprising an "initial program," which necessarily must be loaded to registers), the instructions comprising one or more instructions to initialize the core processing circuit upon release of the core processing circuit from the reset state (column 8, lines 24-26; Anderson discloses an included loader program to download a program from host 11 to FLASH memory, which necessarily must include fetching additional instructions).

Regarding claim 16, Anderson discloses the method of claim 15, wherein the method further comprises transmitting the instructions from the system memory through a host bridge of the host processing system (17).

Regarding claim 17, Anderson discloses the method of claim 15, the method further comprising releasing the core processing circuit from the reset state in response to loading the instructions at the boot address (column 2, lines 37-39).

Regarding claim 18, Anderson discloses the method of claim 15, the method further comprising loading the instructions to a boot address in registers formed in a memory (39) coupled to the core processing circuit (31) through a data bus (26).

Regarding claim 19, Anderson discloses the method of claim 15, wherein the method further comprises setting an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit (column 2, lines 48-50, via processor address bus 24).

Regarding claim 22, Anderson discloses an article comprising: a storage medium comprising machine-readable instructions encoded there on for: having a host processing system place a core processing circuit (13) in a reset state (column 2, lines

65-66; column 3, lines 6-7); and loading a reset vector to one or more registers at a boot address associated with the core processing circuit (column 6, lines 13-15 in view of column 8, lines 7-9; Anderson discloses the reset vector as comprising an "initial program," which necessarily must be loaded to registers), the reset vector comprising one or more instructions to fetch additional instructions from a system memory (column 8, lines 24-26; Anderson discloses an included loader program to download a program from host 11 to FLASH memory, which necessarily must include fetching additional instructions) coupled to the core processing circuit through a host bridge (17) of a host processing system (11).

Regarding claim 23, Anderson discloses the article of claim 22, wherein the storage medium further comprises machine readable instructions stored thereon for loading the reset vector to a boot address in registers formed in a memory (39) coupled to the core processing circuit (31) through a data bus (26).

Regarding claim 24, Anderson discloses the article of claim 22, wherein the storage medium further comprises machine readable instructions stored thereon for setting an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit (column 2, lines 48-50, via processor address bus 24).

Regarding claim 25, Anderson discloses the article of claim 22, wherein the storage medium further comprises machine readable instructions stored thereon for loading the reset vector in the registers while the core processing circuit is in the reset state (column 6, lines 5-7). Anderson does not explicitly disclose initiating of one or

more write bus transactions at an address translation unit, however said transactions would necessarily have to be present in order to properly load the registers.

Regarding claim 26, Anderson discloses the article of claim 22, wherein the storage medium further comprises machine readable instructions stored thereon for releasing the core processing circuit from the reset state in response to loading the reset vector at the boot address (column 2, lines 37-39).

Regarding claim 29, Anderson discloses the article comprising: a storage medium comprising machine-readable instructions encoded there on for: having a host processing system place a core processing circuit (13) in a reset state (column 2, lines 65-66; column 3, lines 6-7); and loading instructions from a system memory of a host processing system to one or more registers at a boot address associated with the core processing circuit (column 6, lines 13-15 in view of column 8, lines 7-9; Anderson discloses the reset vector as comprising an "initial program," which necessarily must be loaded to registers), the instructions comprising one or more instructions to initialize the core processing circuit upon release of the core processing circuit from the reset state (column 8, lines 24-26; Anderson discloses an included loader program to download a program from host 11 to FLASH memory, which necessarily must include fetching additional instructions).

Regarding claim 30, Anderson discloses the article of claim 29, wherein the storage medium further comprises machine readable instructions stored thereon for transmitting the instructions from the system memory through a host bridge of the host processing system (17).

Regarding claim 31, Anderson discloses the article of claim 29, wherein the storage medium further comprises machine readable instructions stored thereon for releasing the core processing circuit from the reset state in response to loading the instructions at the boot address (column 2, lines 37-39).

Regarding claim 32, Anderson discloses the article of claim 29, wherein the storage medium further comprises machine readable instructions stored thereon for loading the instructions to a boot address in registers formed in a memory (39) coupled to the core processing circuit (31) through a data bus (26).

Regarding claim 33, Anderson discloses the article of claim 29, wherein the storage medium further comprises machine readable instructions stored thereon for setting an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit (column 2, lines 48-50, via processor address bus 24).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 13, 20, 27, and 34 rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (U.S. 5,898,869). Said claims are rejected in view of amended claims 1, 9, 15, 22, and 29.

Regarding claims 7, 13, 20, 27, and 34, Anderson discloses all of the limitations of respective independent claims 1, 9, 15, 22, and 29, as noted above. However, though Anderson discloses the additional instructions comprising "diagnostic routines" (column 3, lines 13-14), Anderson does not explicitly disclose the system wherein the additional instructions comprise instructions to commence a power-on self test procedure. The examiner takes Official Notice that power-on self test procedures are a well known type of diagnostic routine. It would have been obvious at the time that the invention was made to use power-on self test procedures for the diagnostic routines disclosed by Anderson. The motivation for doing so would have been to assure the integrity of the information stored on the core processing circuit.

Claims 8, 14, 21, 28, and 35 rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (U.S. 5,898,869) in view of Klein (U.S. 6,226,224). Said claims are rejected in view of amended claims 1, 9, 15, 22, and 29.

Regarding claims 8, 14 and 28, Anderson discloses all of the limitations of respective independent claims 7, 13 and 27 as noted above. However, Anderson does not disclose the method wherein the additional instructions further comprise instructions to launch an operating system to the core processing circuit. Klein teaches a system comprising: a core processing circuit (figure 2, item 106); logic to place the core processing circuit in a reset state (page 2, column 3, lines 25-27); and logic to load a reset vector to one or more registers at a boot address associated with the core processing circuit (page 3, column 5, lines 44-47), the reset vector comprising one or more instructions to fetch additional instructions to initialize the core processing circuit

upon release from the reset state (page 2, column 4, lines 9-13), similar to Anderson. Klein further teaches the method wherein the [additional] instructions further comprise instructions to launch an operating system to the core processing circuit (page 2, column 4, lines 13-15) in order to "bring the PC up to a state that can be used by a human operator" (page 2, column 4, lines 16-17). It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate Klein's teachings of loading the operating system with Anderson's disclosure of a system comprising a core processing circuit initialization with a host processing system. The motivation for doing so would have been to accommodate for the use of the system by a human operator.

Regarding claims 21 and 35, Anderson discloses all of the limitations of respective parent claims 20 and 34, as noted above. However, Anderson does not disclose the method wherein the one or more instructions further comprise instructions to launch an operating system to the core processing circuit. Klein teaches a system comprising: a core processing circuit (figure 2, item 106); logic to place the core processing circuit in a reset state (page 2, column 3, lines 25-27); and logic to load a reset vector to one or more registers at a boot address associated with the core processing circuit (page 3, column 5, lines 44-47), the reset vector comprising one or more instructions to fetch additional instructions to initialize the core processing circuit upon release from the reset state (page 2, column 4, lines 9-13), similar to Anderson. Klein further teaches the method wherein the one or more instructions further comprise instructions to launch an operating system to the core processing circuit (page 2, column 4, lines 13-15) in order to "bring the PC up to a state that can be used by a

human operator" (page 2, column 4, lines 16-17). It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate Klein's teachings of loading the operating system with Anderson's disclosure of a system comprising a core processing circuit initialization with a host processing system. The motivation for doing so would have been to accommodate for the use of the system by a human operator.

Response to Arguments

4. All rejections of claim limitations as filed prior to Amendment dated February 17, 2005 not argued in their entirety or substantively in the response to the prior Office action have been conceded by Applicants and the rejections are maintained from henceforth.

Applicants' arguments filed February 17, 2005 have been fully considered but they are not persuasive.

With regards to the assertions of Anderson's failure to disclose element (b1) of Applicants' claim 1, "[the host processing system comprising] logic to place the core processing circuit in a reset state," element (a) of Applicants' claims 9 and 15, "having a host processing system place a core processing circuit in a reset state," and element (b) of Applicants' claims 22 and 29, "having a host processing system place a core processing circuit in a reset state," the Examiner directs Applicants to Anderson column 2, lines 64-66, which discloses: "The method includes resetting the PCMCIA card, wherein the resetting suspends execution of the processor," in view of Anderson column 3, lines 6-7 of Anderson, which further discloses: "The resetting may also comprise the

host sending a software reset signal." Therefore, the hardware within the host-processing system (item 11 of Anderson) is used to reset the core processing circuit (item 31 of Anderson), as claimed by Applicants' independent claims 1, 9, 15, 22, and 29, and Anderson is a proper basis for a 35 U.S.C. 102(b) rejection.

Accordingly, Applicants' assertions concerning the rejections of dependent claims 2-8, 10-14, 16-21, 23-28 and claims 30-35 are invalid, as the rejections of their respective independent claims 1, 9, 15, 22, and 29 are proper.

Further, Applicants' assertions concerning the rejections of dependent claims 7, 13, 20, 27, and 34 under 35 U.S.C. 103(a), based on the teachings of Anderson, are invalid, as the rejections of their respective independent claims 1, 9, 15, 22, and 29 are proper.

Finally, Applicants' assertions concerning the rejections of dependent claims 8, 14, 21, 28, and 35 under 35 U.S.C. 103(a), based on the combined teachings of Anderson and Klein, are invalid, as the rejections of their respective independent claims 1, 9, 15, 22, and 29 are proper.

Conclusion

5. Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edward K. Park whose telephone number is (571) 272-5859. The examiner can normally be reached on M-F, 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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